

Design of Fluorescent Lamp Ballast With PFC Using a Power Piezoelectric Transformer

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Abstract—An investigation of a high-power piezoelectric transformer (PT) as a potential component for a fluorescent lamp (FL) ballast with power factor correction (PFC) is discussed. The attractiveness of the PT is primarily the simplicity of the resulting circuit, and it is easy to be produced in mass with a low cost. A single-stage charge-pump PFC ballast using a PT is proposed. The proposed ballast circuit improved the drawbacks of the conventional voltage-source charge-pump PFC (VS-CPPFC) scheme. Empirical PT modeling based on power level excitation is performed to design the proposed circuit, and the experimental and simulation results are provided to verify theoretical analysis.

Index Terms—Ballast, charge pump, piezoelectric transformer (PT), power factor correction (PFC).

I. INTRODUCTION

THE PIEZOELECTRIC transformer (PT) is an electro-mechanical device that transfers electrical energy through a mechanical vibration. It features high voltage gain, high power density, compact size, and no electromagnetic noise. Since proposed by Rosen in the 1950s, quite a few papers have proposed the applications with different PTs [1], [2]. Recently, the applications of the PT have extended to the power level of more than 20 W in direct current (dc)–dc converters [3]–[6].

In this paper, a PT operating in the contour vibration mode is introduced for the application to the fluorescent lamp (FL) ballast. Utilizing its inherent resonant characteristic and a high voltage gain to ignite the lamp in light load condition, an FL ballast using the PT, to eliminate the magnetic component, is suggested. The PT is easy to be produced in mass, which reduces the cost of the ballast. When the PT is integrated into a single-stage power factor correction (PFC) FL ballast—the charge-pump PFC circuit [7], the scheme reduces the number of components of the ballast circuit.

In Section II, modeling of the PT, taking into account the power level excitation, is discussed. In Section III, various ballast schemes employing the PT are presented. Experimental results are presented in Section IV.

II. MODELING AND ANALYSIS OF PT

Fig. 1(a) shows the structure of the PT used in this paper. The piezoelectric material is lead zirconate titanate (PZT), and it has a primary electrode in the center and a secondary in the outer part. It operates in the contour vibration mode, and the mechanical resonant frequency is around 75 kHz. The square plate PT sample vibrates laterally, which is perpendicular to the applied electric field, thus, it is referred to as operating in contour extensional vibration mode as defined in [16], and its vibration mode and direction are shown in Fig. 1(b). The turns ratio of the PT is determined mainly by the ratio of the area formed by the primary electrodes to that of the secondary electrodes and also by the dielectric, mechanical, and piezoelectric constants of the material [14]. The gain curve of the PT shows resonant bandpass characteristics, which is dependent on the load condition and is usually provided by the vendor of the PT. It provides a high voltage gain in the light load condition.

An electrical equivalent circuit of the PT around the frequency range of interest can be represented by a resonant bandpass circuitry, as shown in Fig. 2. Its circuit parameter values are calculated through several two-port measurement techniques—admittance circle measurements [9] and s-parameter measurements [10], which may be performed in the signal level. The circuit parameters in the model for the PT are measured and calculated as follows: $L_o = 103.8$ mH; $C_o = 42.9$ pF; $C_1 = 0.593$ nF; $C_2 = 1.98$ nF; and $n = 0.44$. The parameter n represents the electromechanical coupling factor. For the remaining parameter R_o , the empirical determination of the value will be discussed later in this section.

To design the ballast circuit, the electrical equivalent circuit for the PT, which calculates both the steady state and the starting voltage gain, is needed. The electrical circuit model of the PT is established in several papers [8]–[11], but these models did not consider the mechanical quality factor decrement at the power level. Especially in the light load condition, there is too large of an error between the measured and simulated data when signal level measurement is used.

The mechanical part can be modeled by a series resonant branch as in Fig. 3 [8]. Past researchers on piezoelectric materials have reported that, in the power level driving, with an increased mechanical velocity of particles in the piezoelectric structure, the mechanical quality factor decreases [17], and, thus, the PT gain decreases. The mechanical velocity is modeled by the resonant current (i_m) through the branch, and the decrement in the mechanical quality factor can be modeled by an increment of the series resistance R_m . Therefore, R_v is an

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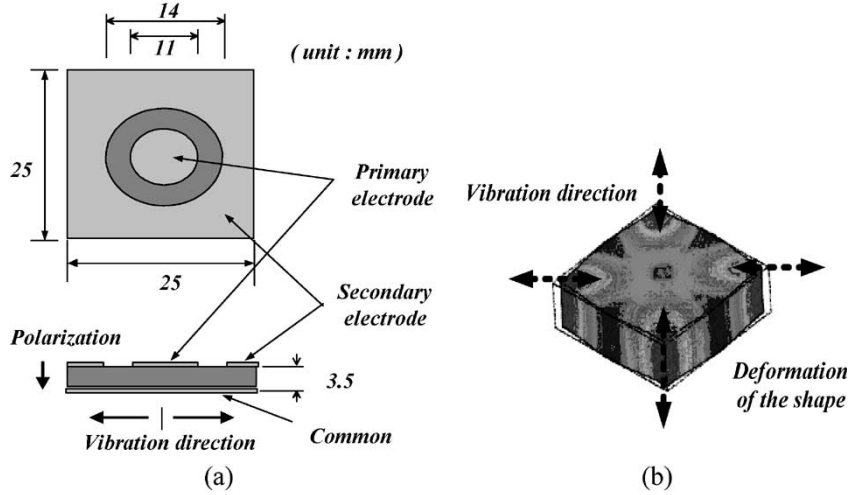


Fig. 1. Physical arrangement of the PT. (a) Dimensions. (b) Vibration directions (contour vibration mode).

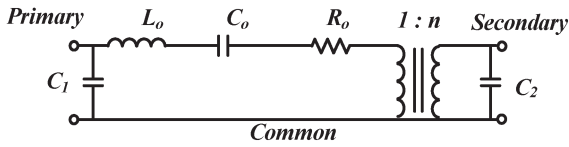


Fig. 2. Conventional circuit model of the PT around the resonant frequency.

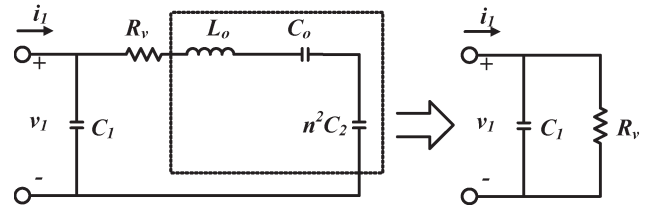


Fig. 4. Equivalent circuit at the resonance frequency in open load condition.

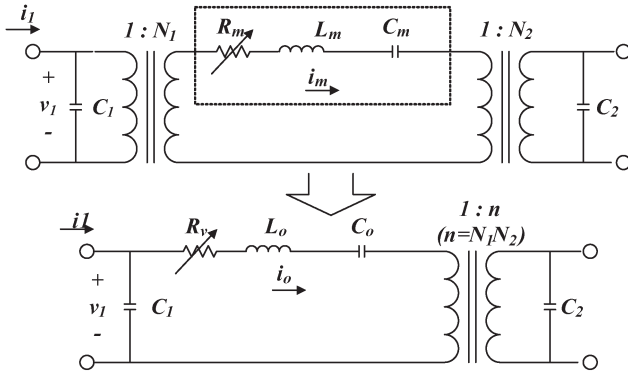


Fig. 3. Modified electrical equivalent model of PT.

increasing function of the internal current flow i_o in Fig. 3. Because the impedance of the C_1 branch is usually higher than the series resonant branch, R_v can be assumed to be a nonlinear increasing function of the PT input current i_1 as in (1)

$$R_v = f(i_1). \quad (1)$$

With this assumption, the value of the internal equivalent resistance of the model can be measured by the following method. Once the load is open, the input impedance of the PT is measured with an operating frequency tuned to the resonant frequency. Using fundamental approximations in the equivalent circuit at the resonance frequency as shown in Fig. 4, the measured input impedance Z_{in} is given by

$$|Z_{in}| = \frac{V_{1rms}}{I_{1rms}} = \left| \frac{1}{j\omega C_1} \parallel R_v \right|. \quad (2)$$

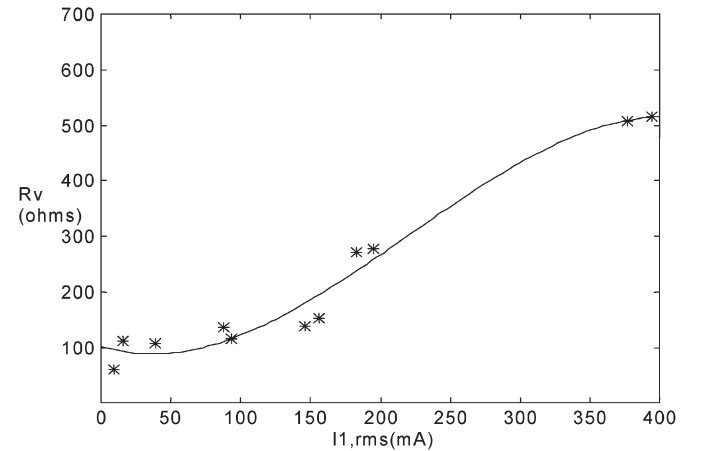


Fig. 5. Curve fitting for R_v .

Then, the internal resistance R_v is calculated by

$$R_v = |Z_{in}| \frac{1}{\sqrt{1 - (\omega |Z_{in}| C_1)^2}}. \quad (3)$$

This calculation is repeated through several input current levels of i_1 . Using a curve-fitting algorithm, (1) is approximated as a third-order polynomial as in Fig. 5, and it is incorporated into a circuit model block of commercial circuit analysis programs such as PSPICE behavioral circuit model of the PT. The flow chart for the model derivation sequence is summarized in Fig. 6.

Fig. 7 compares the measured and simulated open load voltage gain curves of the PT using the constructed circuit model. Fig. 8 shows the voltage gain of the PT as the resistive

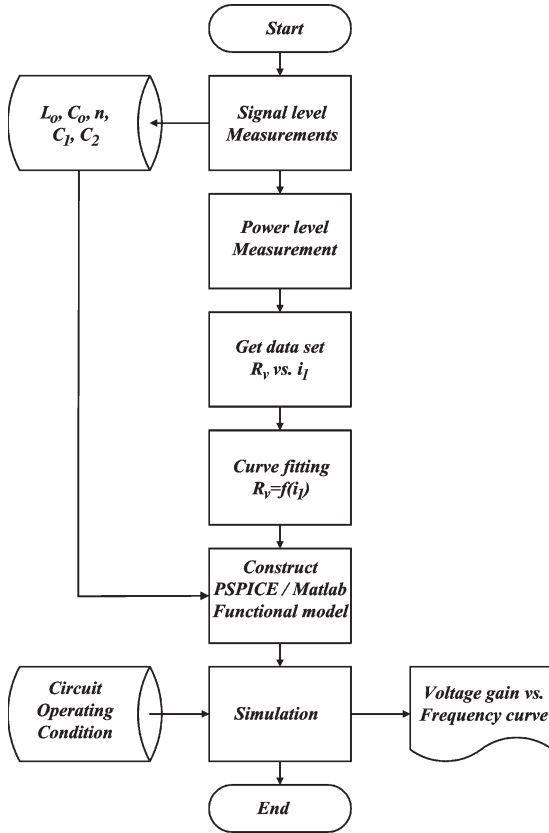


Fig. 6. Flowchart for the model construction.

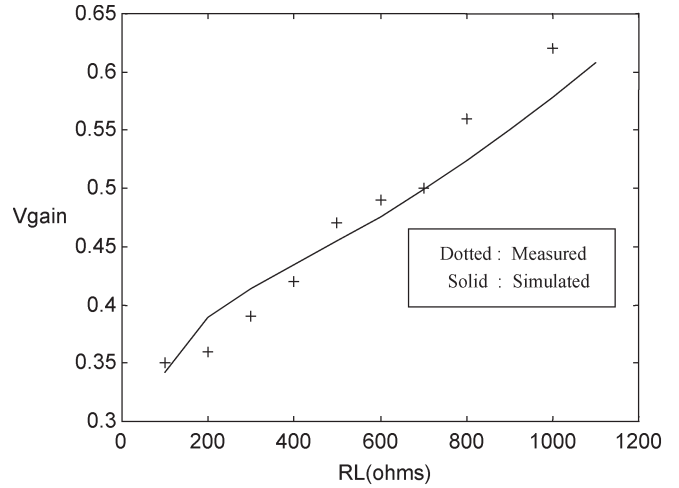


Fig. 8. Maximum voltage gain as resistive load varies.

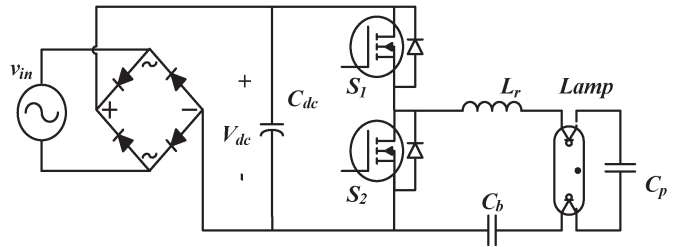


Fig. 9. Conventional ballast.

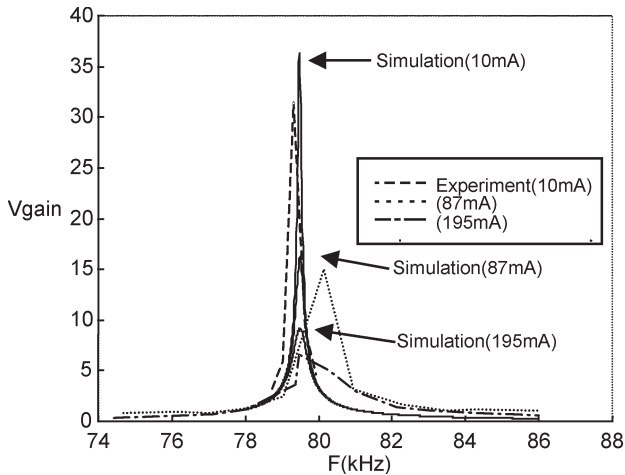


Fig. 7. Open load voltage gain at several current levels.

load varies. It is shown that the simulation model can be used in the voltage gain calculation for the design of the ballast.

III. ELECTRONIC BALLAST USING PTs

Generally, a half-bridge series-parallel resonant inverter, as shown in Fig. 9, is used in the electronic FL ballasts. The inductor (L_r) limits the current and resonates with the shunt capacitor (C_p) to provide a sufficient starting voltage to the lamp. However, this inductor raises the cost and size of the electronic ballast. In this paper, to eliminate the magnetic

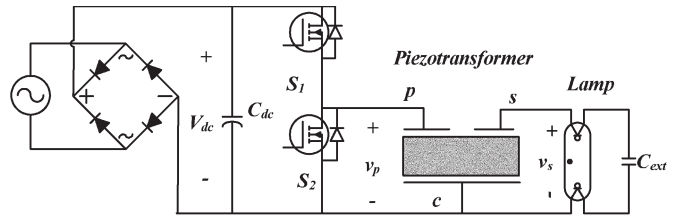


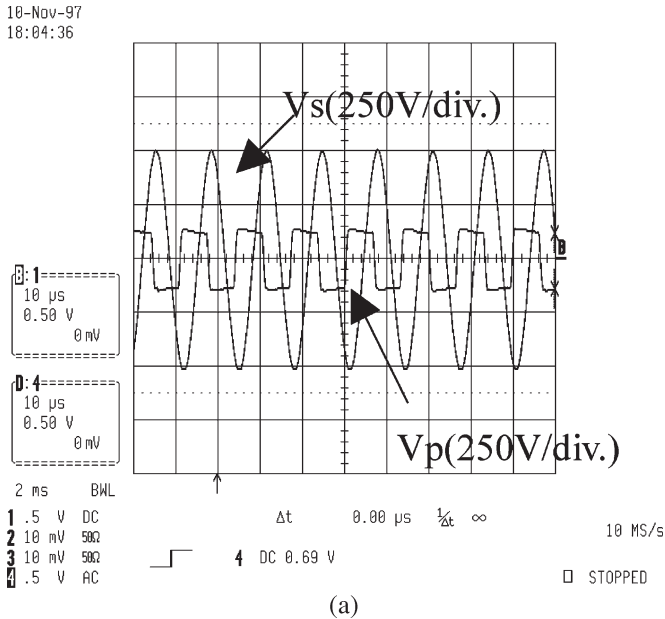
Fig. 10. Low-power PT ballast.

component, FL ballasts using the PT in place of the inductor are suggested.

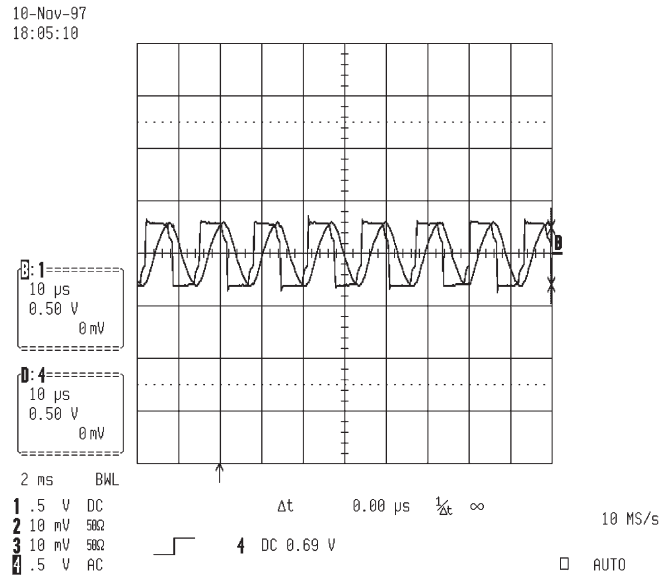
A. Low-Power PT Ballast

In Fig. 10, a low-power PT ballast circuit is presented. As mentioned in the previous section, the PT has a high voltage gain in the light load and a low voltage gain in the heavy load. This characteristic matches well with FL load. Before ignition, the FL has no current path and is modeled by an open circuit. When it ignites, it behaves like a resistor [12]. C_{ext} provides the preheating current path to the rapid-start FL. In order to provide a sufficient preheating current, $C_{ext} = 2.2 \text{ nF}$ is used.

When a square voltage waveform is applied to the primary part of the PT, from the inherent resonant characteristics, the output waveform of the PT is sinusoidal, as in Fig. 11. Furthermore, the output voltage is dependent on the load impedance. Using the model developed in the previous section, the voltage gain curve is generated as shown in Fig. 12. For



(a)



(b)

Fig. 11. PT primary and secondary voltage. (a) Start-up phase. (b) Steady phase.

the steady-state operating condition, a 12 W equivalent lamp load of 800 $[\Omega]$ is used for the simulation. The ignition voltage should be about $500V_{\text{peak}}$, whereas a steady state voltage of $100V_{\text{rms}}$ is needed. The required voltage gain of the PT is calculated as 2.5 for an ignition and 0.71 for a steady state, which are derived in Appendix A. Therefore, in Fig. 12, an operating frequency of 77.2 kHz is chosen.

Fig. 13 shows the steady state lamp current and voltage waveforms. Because of the high- Q characteristics of the PT, the waveforms are near sinusoidal, and the crest factor of the lamp current is very low.

B. High-Power PT Ballast With Charge-Pump PFC

Nowadays, the increasing demand for the input line current regulation to meet the total harmonic distortion (THD) spec-

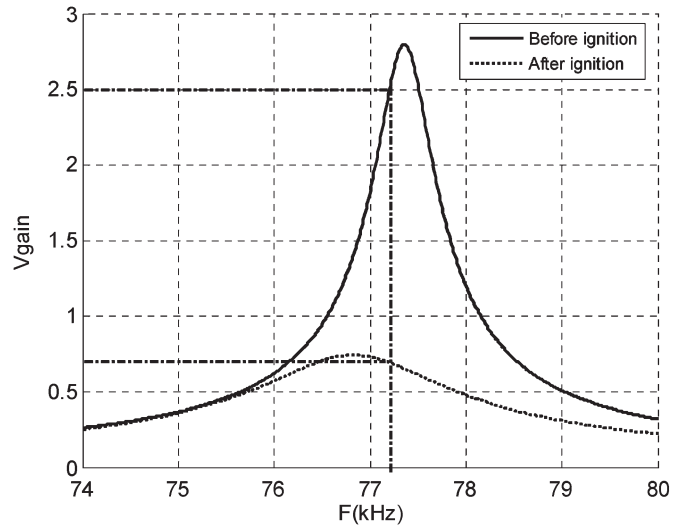


Fig. 12. Voltage gain curve of the PT with $C_{\text{ext}} = 2.2$ nF.

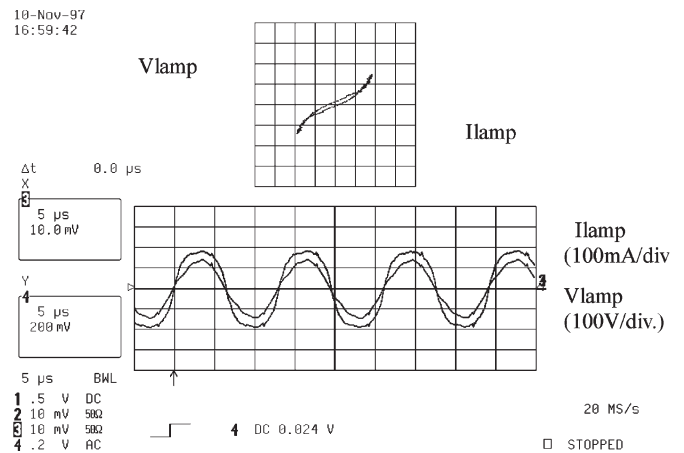


Fig. 13. 12.5 W PT compact FL ballast.

ification such as IEC61000-3-2 is an important issue in the power electronics field. As the operating power increases, the electronic ballast may require a PFC.

Due to the input capacitance C_1 of the PT, when the square voltage waveform is directly applied to the PT, the high peak current flows through the switches, and for the reduction of this current, a small inductor (L_r) is needed. This is especially necessary for the high-power ballast for which a multilayer structure is adopted for the higher power capacity of the PT. The inductor resonates with the PT input capacitor to produce a sinusoidal voltage waveform in the primary part of the PT. However, if the input voltage of the PT increases too much, the isolation between the primary and secondary electrodes may be broken. For the sample used for this design, it is necessary to limit the driving voltage to V_{dc} , about 400 V, by the diode clamps (D_1 and D_2) as shown in Fig. 14. The voltage waveforms of the driving circuit are shown in Fig. 15.

Fig. 16(b) shows the diode-clamped PT ballast implemented to the charge-pump PFC [7]. From the derivations in

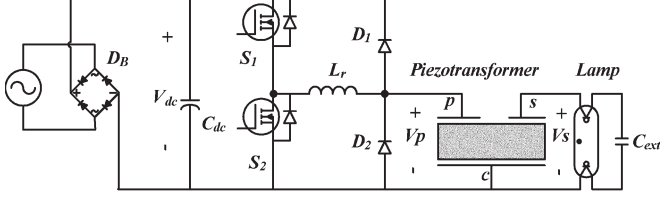


Fig. 14. Diode clamping technique in PT.

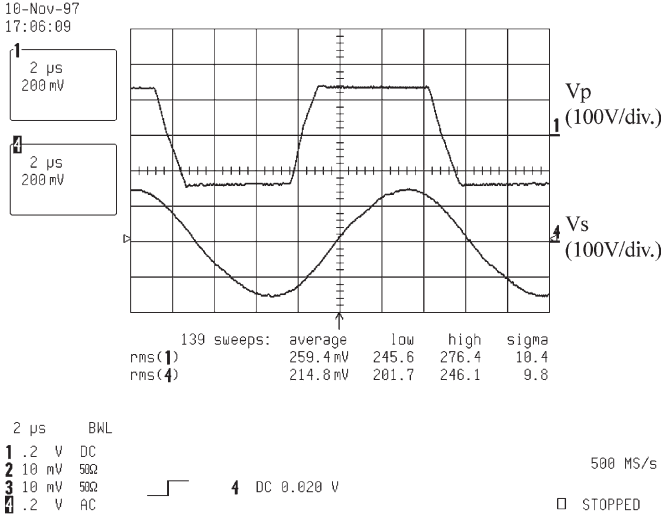


Fig. 15. PT primary and secondary voltage waveforms.

Appendix A, the unity power factor condition in the charge-pump PFC circuit is

$$2V_{p,mag} = V_{dc}. \quad (4)$$

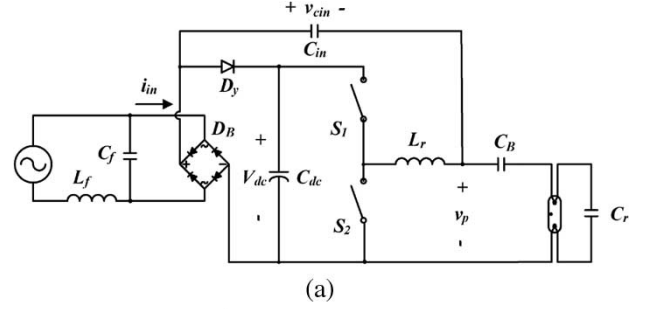
In this condition, the average input current follows the line voltage as

$$|i_{in}| = i_{in,avg} = f_s C_{in} |V_{in}| \propto |V_{in}|. \quad (5)$$

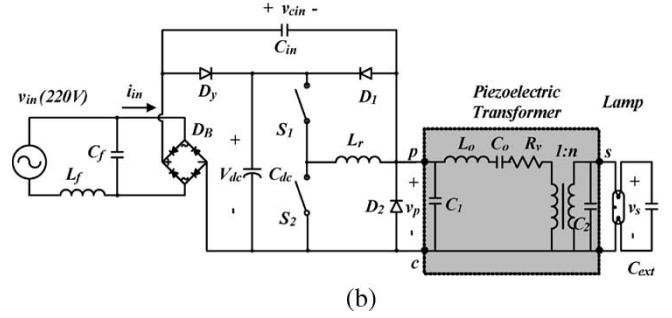
By adopting clamping diodes in the PT primary, condition (4) is achieved. The average input current is directly proportional to line input voltage as in (5). This implies that the proposed circuit shows a good power factor.

The conventional basic voltage-source charge-pump PFC (VS-CPPFC) ballast in Fig. 16(a), which was originally proposed in [7], has two drawbacks, namely: 1) a charge capacitor C_{in} modulation effect; and 2) a high dc bus voltage in the lamp preheat and start-up phase. The former is due to the fact that C_{in} is in parallel with the shunt capacitor C_r when the bridge diode D_B or the discharging diode D_y is on, and the equivalent resonant capacitor changes over one line cycle, which directly deteriorates the lamp crest factor. In the start-up phase, the lamp voltage is more than three times the normal operating voltage and increases dc bus voltage up to 900 V [15].

However, in the proposed PT ballast, C_{in} is not a factor directly determining the PT output, because the lamp voltage is developed by the PT gain. Though the C_{in} modulation affects the PT primary voltage V_p , the PT output is a pure sine waveform, which lowers the lamp crest factor. Moreover, an



(a)



(b)

Fig. 16. Charge-pump PFC ballasts for higher lamp power. (a) Conventional VS-CPPFC ballast. (b) Proposed fluorescent lamp ballast with PFC using PT.

inherent high gain of the PT maintains a low primary voltage even in the light load of the lamp start-up phase, in which the dc bus voltage does not increase above 400 V.

The design equations for C_{in} and L_r are derived using the power balance condition in Appendix A and are obtained as

$$C_{in} = \frac{P_{out}}{\eta f_s V_{in,rms}^2} \quad (6)$$

$$L_r = \frac{(1 - \cos 2\pi D_{eff})}{4\pi^2 C_{in} f_s^2}. \quad (7)$$

IV. EXPERIMENTAL RESULTS

The hardware experiments were carried out with the proposed charge-pump PFC ballast for a compact FL (OSRAM Dulux EL 20W/21). The input line is from 220 V mains and the operating frequency is fixed to 77.2 kHz. Substituting $f_s = 77.2$ kHz, $D_{eff} = 0.25$, $P_o = 18$ W, $\eta = 70\%$, and $V_{p,mag} = \sqrt{2} \times 220$ V in the design equation, we calculated $C_{in} = 6.72$ nF and $L_r = 644$ μ H using (6) and (7) and implemented the hardware with $C_{in} = 6.8$ nF and $L_r = 650$ μ H.

Fig. 17 shows the experimental waveforms. Fig. 18 shows the waveforms of the line input current and voltage of the ballast. A power factor of 0.99 and THD of 10% was obtained. The starting behavior of the lamp is in Fig. 19, where the current crest factor is very low. It operates in the fixed operating frequency, and it does not provide the optimal preheat time condition [13]. It is, however, possible to change the preheat time by adopting the frequency control described in Appendix B. The steady state lamp voltage and current are shown in Fig. 20. Overall efficiency from the input line to the output lamp is 70% with an 18 W output power. This is mainly due to the fact that the efficiency of the current PT sample is about 85%. The structure of a square shape shows some spurious

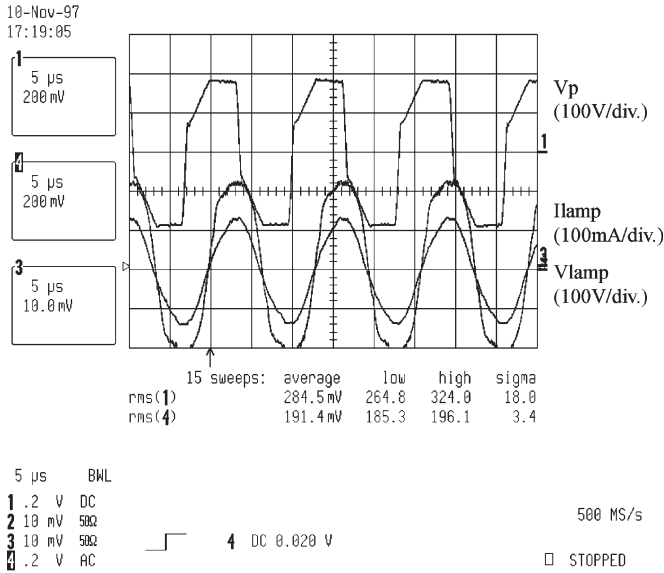


Fig. 17. Waveforms of the charge-pump PFC PT ballast.

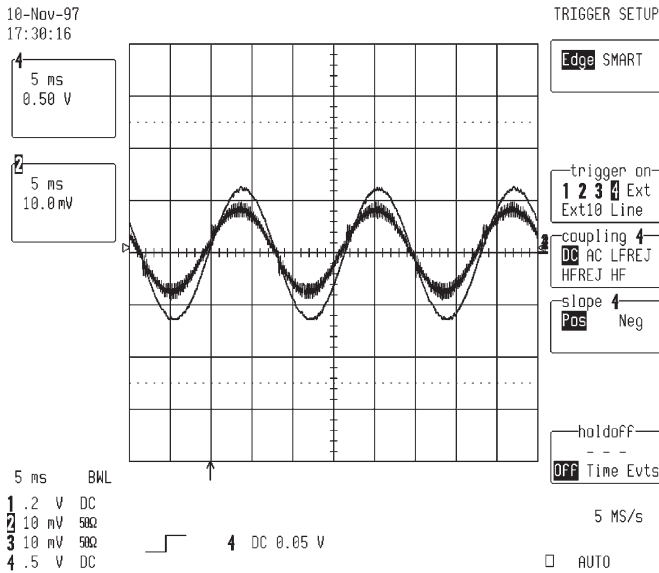


Fig. 18. Line current (200 mA/div) and line voltage (250 V/div).

vibration modes, which generates additional loss in the PT. The efficiency can be improved by adopting a disk-shaped PT, which is currently under development and is analyzed in [14].

V. CONCLUSION

The equivalent model of a piezoelectric transformer (PT) considering power level excitation is derived for the design of a fluorescent lamp (FL) ballast. This model describes the voltage gain of the PT in wide load variations with power applications. Two kinds of FL ballasts using the PT are presented. The PT reduces the number of magnetic components and, thus, the cost. For low-power ballasts, direct replacement of the resonant components by the PT is possible. For high-power ballasts, the charge-pump power factor correction (PFC) FL ballast circuit is presented. The proposed circuit improved the drawbacks of the conventional charge-pump circuit by adding the PT. The power

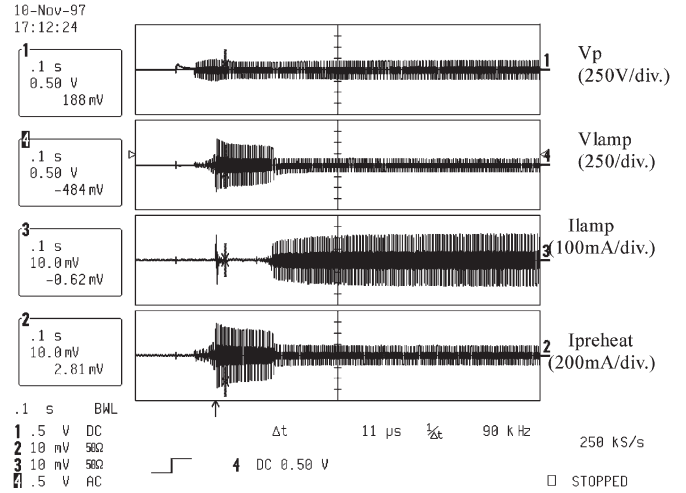


Fig. 19. Starting behavior.

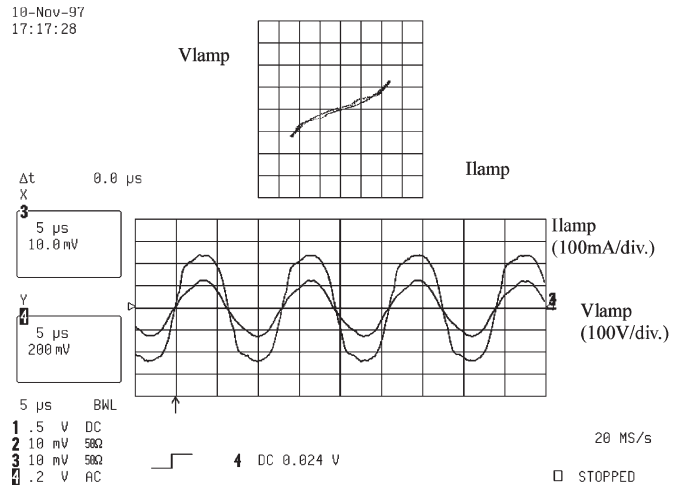


Fig. 20. Steady state lamp voltage and current.

capacity of the currently developed PT is relatively low (18 W), but it can be increased by adopting a multilayer structure and is currently under investigation. It is also possible to parallel the PT for higher power processing.

APPENDIX A

Formula to Calculate R_v for Curve Fitting

Assume an empirical relation of

$$R_m \propto i_m. \quad (A1)$$

This is further simplified in the equivalent circuit in Fig. 3 as

$$i_o = n_1 \times i_m$$

$$R_v = \frac{R_m}{n_1^2} \quad (A2)$$

where n_1 is the electromechanical coupling factor in the primary electrode.

When the sinusoidal current source tuned to the series resonance of the mechanical branch of the equivalent circuit is

applied to the PT samples, the admittance of the capacitance C_1 is much less than that of the mechanical resonance path, and, thus, most of the input current i_1 flows into the resonant path. Therefore, the current through C_1 is negligible by approximation. Therefore, (A1) can be reduced to (1).

Using a fundamental approximation in the equivalent circuit at the resonance frequency shown in Fig. 4, the input impedance is directly given by the parallel combination of C_1 and the resonant branch. The measured input impedance Z_{in} with open load is given by (2)

$$|Z_{in}| = \frac{V_{1rms}}{I_{1rms}} = \left| \frac{1}{j\omega C_1} \parallel R_v \right|. \quad (A3)$$

Equation (3) for R_v is obtained by rearranging the above equation. From measured V_{1rms} , I_{1rms} , resonant frequency, and C_1 , the value of R_v can be calculated.

Required Voltage Gain in the Ballast Design

Let the ac line be $220 V_{ac}$ and $220 \times \sqrt{2}$ is the dc-link voltage (V_{dclink}). From the harmonic approximation analysis, the fundamental rms value of the PT input voltage is given by

$$V_{p,fund,rms} = V_{dclink} \times \frac{2}{\pi} \times \frac{1}{\sqrt{2}}. \quad (A4)$$

For an ignition of the lamp, the minimum start-up voltage should be about $500V_{peak}$. From the minimum starting voltage condition, the minimum required voltage gain of the PT during the ignition phase is obtained as

$$V_{gain,starting} \approx \frac{500}{\frac{\sqrt{2}}{V_{p,fund,rms}}} = 2.5. \quad (A5)$$

Once the lamp is ignited, a steady state voltage of $100V_{rms}$ is needed to sustain the lamp operation, thus, the steady state gain of the PT should be

$$V_{gain,ss} \approx \frac{100}{V_{p,fund,rms}} = 0.71. \quad (A6)$$

PFC Condition

For a VS-CPPFC circuit, active PFC is accomplished by the charging and discharging of the charge-pump capacitor C_{in} . From [15], the capacitor is charged to

$$V_{cin,max} = V_{p,mag} + |v_{in}| \quad (A7)$$

where $V_{p,mag}$ is the peak voltage of the primary side of the PT and V_{dc} is the dc bus voltage and is discharged to

$$V_{cin,min} = V_{dc} - V_{p,mag}. \quad (A8)$$

The charging current through C_{in} is supplied by the ac line and the discharge current is delivered to the dc bus capacitor. Therefore, the average ac current over one switching cycle equals the average charging current of C_{in} . The charge variation is

$$\Delta Q = C_{in}(V_{cin,max} - V_{cin,min}). \quad (A9)$$

By substituting $V_{cin,max}$ and $V_{cin,min}$ into the above equation, the average rectified line current in a switching cycle is given by

$$|i_{in}| = i_{in,avg} = \Delta Q f_s = C_{in} f_s (|v_{in}| + 2V_{p,mag} - V_{dc}). \quad (A10)$$

In order to achieve unity power factor, it is required that the line input current is directly proportional to the input voltage. From (A10), if the circuit is designed such that

$$2V_{p,mag} = V_{dc} \quad (A11)$$

then the rectified line current is

$$|i_{in}| = i_{in,avg} = f_s C_{in} |V_{in}| \propto |V_{in}|. \quad (A12)$$

Thus, the input current follows the line voltage, so the unity power factor can be obtained.

Derivation of the Design Equation for C_{in} and L_r

The design equations are derived using the power balance equation. The input power during the half line cycle has to be equal to the output power. From (A12), the input power during the half cycle is given by

$$P_{in} = \frac{2}{T_L} \int_0^{\frac{T_L}{2}} |i_{in}| |v_{in}| dt = \frac{2}{T_L} \int_0^{\frac{T_L}{2}} C_{in} f_s |v_{in}|^2 dt = \frac{P_{out}}{\eta} \quad (A13)$$

where η is the circuit efficiency and T_L is the period of ac line input voltage. It can be arranged to be

$$C_{in} f_s (V_{in,rms})^2 = \frac{P_{out}}{\eta} \quad (A14)$$

and the design equation for C_{in} is obtained as

$$C_{in} = \frac{\frac{P_{out}}{\eta}}{f_s V_{in,rms}^2}. \quad (A15)$$

The current through the charge-pump capacitor $i_{C_{in}}$, is shown in Fig. 21. Only the positive charging period in the current $i_{C_{in}}$ corresponds to the line input current, thus, it can be approximated by

$$i_{in} = \frac{|v_{in}|}{Z_o} \sin(\omega_o t) \quad (0 \leq t \leq D_{eff} T_s)$$

$$Z_o = \sqrt{\frac{L_r}{C_{in}}}$$

$$\omega_o = \frac{1}{\sqrt{L_r C_{in}}} \quad (A16)$$

where D_{eff} is defined as the charging current duty in the charge-pump PFC capacitor C_{in} and is also shown in Fig. 21.

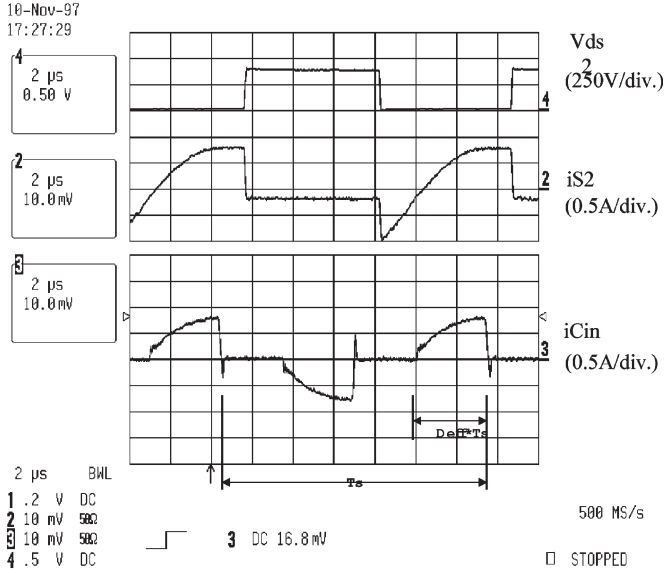


Fig. 21. Waveforms of the charge-pump PFC PT ballast.

Thus, the average input current in one switching period is given by

$$i_{in,avg} = \frac{1}{T_s} \int_0^{D_{eff}T_s} \frac{|v_{in}|}{Z_o} \sin \omega_0 t dt$$

$$= \frac{|v_{in}|}{2\pi Z_o} (1 - \cos 2\pi D_{eff}). \quad (A17)$$

By equating (A15) and (A17), L_r is obtained as

$$L_r = \frac{(1 - \cos 2\pi D_{eff})}{4\pi^2 C_{in} f_s^2}. \quad (A18)$$

APPENDIX B

Control Issues of PT With Respect to Temperature and Mass Production Tolerance

If the temperature increases, the voltage gain of the PT slightly increases, and the center frequency of the bell-shaped gain curve slightly moves to the right. Moreover, the vendor of the PT sample, Dong-il Tech, reported that there is a tolerance of about 2% in the peak voltage gain frequency and 10% in gain in mass production. To handle these problems, a lamp current control loop should be implemented with the PT ballast as shown in Fig. 22(a). Deviations in the frequency and gain can be automatically tracked by changing the gate pulse frequency to generate the required gain.

Improvement of the Lamp Preheating Scheme

The preheat time can be optimally designed using the frequency control scheme with a timer circuit. As shown in Fig. 22(b), the soft-start timer circuit maintains the operating frequency ($f_{preheat}$) higher than the lamp ignition frequency (f_{normal}). Once the lamp is ignited, the current loop begins to operate.

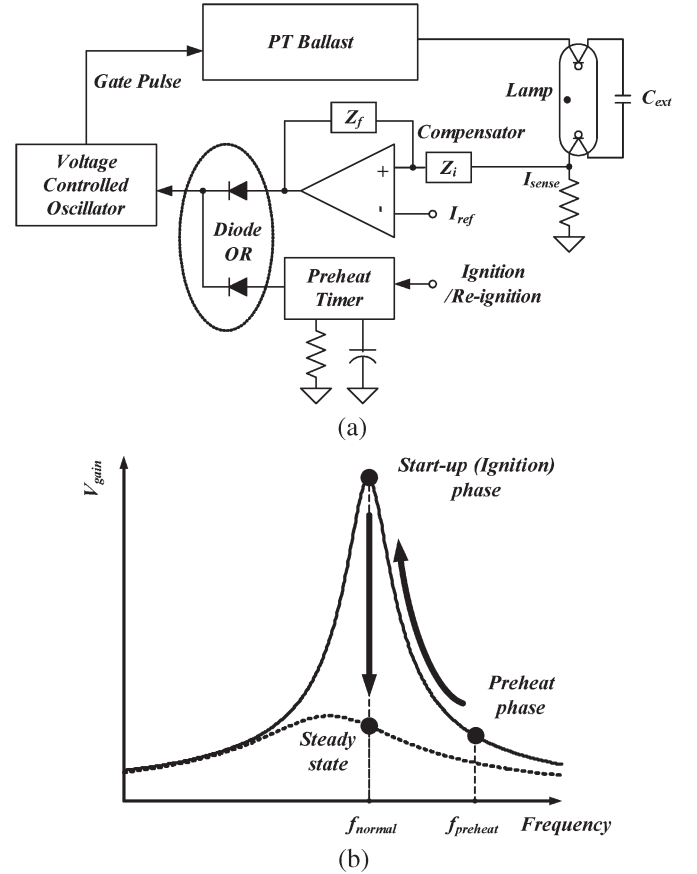


Fig. 22. Frequency control scheme to regulate the output current and to improve the preheat condition.

through the external capacitance C_{ext} . After a preheat time, the operating frequency decreases to the ignition frequency (f_{normal}). Once the lamp is ignited, the current loop begins to operate.

REFERENCES

- [1] C. Y. Lin and F. C. Lee, "Piezoelectric transformer and its applications," in *Proc. VPEC Conf.*, Blacksburg, VA, 1995, pp. 129–136.
- [2] M. Shoyama, K. Horikoshi, T. Ninomiya, T. Zaitzu, and Y. Sasaki, "Operational analysis of the push-pull piezoelectric inverter," in *Conf. Rec. IEEE Applied Power Electronics Conf. (APEC)*, Vancouver, BC, Canada, 1997, pp. 573–578.
- [3] T. Zaitzu, T. Inoue, O. Ohnishi, and A. Iwamoto, "2 MHz power converter with piezoelectric ceramic transformer," in *Proc. IEEE Int. Telecommunications Energy Conf. (INTELEC)*, Washington, DC, 1992, pp. 430–437.
- [4] T. Zaitzu, O. Ohnishi, T. Inoue, M. Shoyama, T. Ninomiya, F. C. Lee, and G. C. Hua, "Piezoelectric transformer operating in thickness extensional vibration and its application to switching converter," in *Conf. Rec. IEEE Power Electronics Specialists Conf. (PESC)*, Taipei, Taiwan, R.O.C., 1994, pp. 585–589.
- [5] T. Zaitzu, T. Shigehisa, M. Shoyama, and T. Ninomiya, "Piezoelectric transformer converter with PWM control," in *Conf. Rec. IEEE Applied Power Electronics Conf. (APEC)*, San Jose, CA, 1996, pp. 279–283.
- [6] C. Y. Lin and F. C. Lee, "Design of piezoelectric transformer converters using single-ended topologies," in *Proc. VPEC Conf.*, Blacksburg, VA, 1994, pp. 107–112.
- [7] W. Chen and F. C. Lee, "An improved charge pump electronic ballast with low THD and low crest factor," in *Conf. Rec. IEEE Applied Power Electronics Conf. (APEC)*, San Jose, CA, 1996, pp. 622–627.
- [8] H. W. Katz, *Solid-State Magnetic and Dielectric Devices*. New York: Wiley, 1959.

- [9] P. J. M. Smidt and J. L. Duarte, "Powering neon lamps through piezoelectric transformers," in *Conf. Rec IEEE Power Electronics Specialists Conf. (PESC)*, Baveno, Italy, 1996, pp. 310–315.
- [10] C. Y. Lin and F. C. Lee, "Design of a piezoelectric transformer converter and its matching networks," in *Power Electronics Specialists Conf. (PESC) Rec.*, Taipei, Taiwan, 1994, pp. 607–612.
- [11] Y. Kaname and Y. Ise, "A study of transducer design of piezoelectric ceramic transformers," *J. Acoust. Soc. Jpn.*, vol. 32, no. 8, pp. 470–474, Aug. 1975.
- [12] P. R. Herrick, "Mathematical models for high intensity discharge lamps," *IEEE Trans. Ind. Appl.*, vol. COMM-16, no. 5, pp. 648–654, Sep./Oct. 1980.
- [13] Y. Ji and R. Davis, "Starting performance of high-frequency electronic ballasts for 4-foot fluorescent lamps," in *Conf. Rec. IEEE Industry Applications Conf. (IAS) Annu. Meeting*, Orlando, FL, 1995, pp. 2083–2089.
- [14] S. J. Choi, T. I. Kim, S. M. Lee, and B. H. Cho, "Modeling and characterization of radial-mode disk-type piezoelectric transformer for AC/DC adapter," in *Conf. Rec Power Electronics Specialists Conf. (PESC)*, Recife, Brazil, 2005, pp. 624–629.
- [15] J. Qian, "Advanced single-stage power factor correction techniques," Ph.D. dissertation, Dept. Elect. Eng., Virginia Polytechnic Inst. State Univ., Blacksburg, 1997.
- [16] "IRE standards on piezoelectric crystals: Determination of the elastic, piezoelectric, and dielectric constants—the electromechanical coupling factor," *Proc. IRE*, vol. 46, no. 4, pp. 764–778, Apr. 1958.
- [17] S. Takahashi, S. Hirose, K. Uchino, and K.-Y. Oh, "Electro-mechanical characteristics of lead-zirconate-titanate ceramics under vibration-level change," in *Conf. Rec. Proc. IEEE Int. Symp. Applications Ferroelectrics*, University Park, PA, 1994, pp. 377–382.



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